Large Current External FET Controller Type Switching Regulator

Dual-output High-frequency step-down Switching Regulator (Controller type)

BD9842FV

● Overview

BD9842FV is an IC containing two circuits of switching regulator controller by pulse width modulation system.
Both of two circuits can be used for step-down DC/DC converter operation.
In addition, the package is designed compact, and is optimum for compact power supply for many kinds of equipment.

● Feature

1) High voltage resistance input (Vcc=35V)
2) FET driver circuit is contained (step-down circuit 2 output).
3) Error amplifier reference voltage (1.0V±1%) and REG output circuit (2.5V) are contained.
4) Overcurrent detection circuit is contained.
5) Soft start and pause period can be adjusted.
6) Three modes of standby, master, and slave can be switched. (iccs = 0 uA typ in standby mode.)
7) ON/OFF control is enabled independently for each channel. (DT terminal)

● Application

LCD, PDP, PC, AV, Printer, DVD, Projector TV, Fax, Copy machine, Measuring instrument, etc.

● Operating condition (Ta=25°C)

Item	Symbol	Range	Unit
Supply voltage	Vcc	3.6 to 35	V
Output terminal voltage	OUT	C5V – Vcc	V
Timing capacity	CCT	47 to 3000	pF
Oscillation frequency	Fosc	100 to 1500	kHz
STB input voltage	STB	0 to Vcc	V

● Absolute maximum rating

Item	Symbol	Rating	Unit
Supply voltage	Vcc	36	V
Permissible loss	Pd	812*1	mW
OUT terminal voltage resistance	OUT	Vcc-7V to Vcc	V
C5V terminal voltage resistance	C5V	Vcc-7V to Vcc	V
Operation temperature range	Topr	-40 to +105	°C
Storage temperature range	Tstg	-55 to +150	°C
Joint temperature	Tjmax	150	°C

*1 When glass epoxy board 70.0 mm × 70.0 mm × 1.6 mm is installed onboard. Reduced by 6.5 mW/C above Ta=25°C.

Sep. 2008

●Electric characteristics (Ta25°C, VCC=6V unless otherwise specified)

Item	Symbol	Standard value			Unit	Condition
		Minimum	Standard	Maximum		
[VREF output unit]						
Output voltage	V_{REF}	2.450	2.500	2.550	V	I_O=0.1 mA
Input stability	Line reg.	—	1	10	mV	Vcc=3.6 V→35 V
Load stability	Load reg.	—	2	10	mV	I_O=0.1 mA→2 mA
Current capacity	I_{OMAX}	2	13	—	mA	V_{REF}=(typ.)∗0.95
[Triangular wave oscillator]						
Oscillation frequency	F_{OSC}	95	106	117	kHz	C_{CP}=1800 pF
Frequency fluctuation	F_{DV}	—	0	1	%	Vcc=3.6 V→35 V
CT source current	I_{CTSO}	190	200	210	μA	CT=1.75 V
CT sink current	I_{CTSI}	190	200	210	μA	CT=1.75 V
[Soft start unit]						
SS source current	I_{SSSO}	1.4	2	2.6	μA	SS=0.5 V
SS sink current	I_{SSSI}	5	12	—	mA	SS=0.5 V
[Pause period adjusting circuit]						
DT input bias current	I_{DT}	—	0.1	1	μA	DT=1.75 V
DT sink current	I_{DTSI}	1	3.3	—	mA	DT=1.75 V, (OCP+)-(OCP-)=0.5 V
[Low input malfunction preventing circuit]						
Threshold voltage	V_{UTH}	3.0	3.2	3.4	V	Vcc start detection
Hysteresis	V_{UHYS}	—	0.15	0.25	V	
[Error amplifier]						
Non-inverting input reference voltage	V_{INV}	0.99	1	1.01	V	INV=FB
Reference voltage supply fluctuation	dVinv	—	1	6	mV	Vcc=3.6 V→35 V
INV input bias current	I_{IB}	—	0	1	μA	INV=1 V
Open gain	AV	70	85	—	dB	
Max output voltage	V_{FBH}	2.30	—	VREF	V	
Min output voltage	V_{FBL}	—	0.6	1.3	V	
Output sink current	I_{FBSI}	0.5	1.5	—	mA	FB=1.25 V, INV=1.5 V
Output source current	I_{FBSO}	50	105	—	μA	FB=1.25 V, INV=0.5 V
[PWM comparator]						
Input threshold voltage （fosc=100kHz）	V_{t0}	1.4	1.5	1.6	V	On duty 0%
（fosc=100kHz）	V_{t100}	1.9	2	2.1	V	On duty 100%
[Output unit]						
Output ON resistance H	R_{ONH}	—	4.0	10	Ω	R_{ONH}=(V_{CC} -OUT)/ Iout, Iout=0.1 A
Output ON resistance L	R_{ONL}	—	3.3	10	Ω	R_{ONL}=(OUT-C5 V)/ Iout, Iout=0.1 A
C5V clamp voltage	V_{CLMP}	4.5	5	5.5	V	V_{CLMP}= V_{CC}-C5V , V_{CC} ＞7 V
[Overcurrent protection circuit]						
Overcurrent detection threshold voltage	V_{OCPTH}	0.04	0.05	0.06	V	Voltage between (OCP+) and (OCP-)
OCP-input bias current	I_{OCP-}	—	0.1	10	μA	OCP+= V_{CC}, OCP-= V_{CC}-0.5 V
Overcurrent detection delay time	tdocpth	—	200	400	nS	OCP-= V_{CC}→V_{CC}-0.2 V
Overcurrent detection minimum retention time	tdocpre	0.8	1.6	—	mS	OCP-= V_{CC}-0.2 V→V_{CC}

[Standby changeover unit]						
Single channel stop threshold voltage	V_{DTthL}	1.1	1.25	1.4	V	DT terminal H/L
Standby mode setting range	V_{STBL}	0	—	0.5	V	
Slave mode setting range	V_{STBM}	2.4	2.5	2.6	V	
Active (master) mode setting range	V_{STBH}	3	—	V_{CC}	V	
STB flow-in current	I_{STB}	—	70	100	μA	STB=6 V
[Device overall]						
Standby current	I_{CCS}	—	0	1	μA	STB=0 V
Average power consumption	I_{CCA}	1.5	3	6	mA	INV=0 V, FB=H, DT=1.75 V

* Radiation resistance design is not applied.

●Reference data

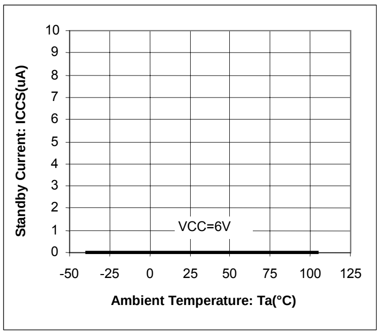


Fig.1 Standby current temperature characteristics

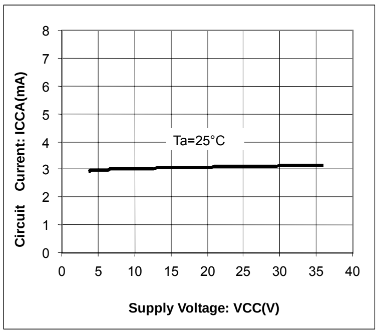


Fig.2 Circuit current in operation

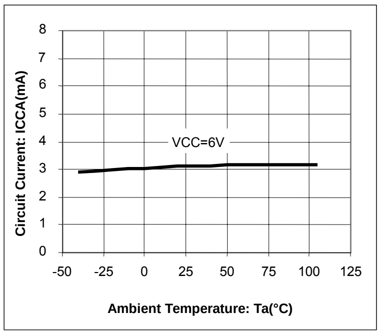


Fig.3 Circuit current temperature characteristics in operation

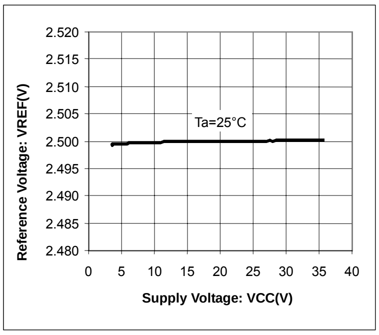


Fig.4 VREF supply voltage characteristics

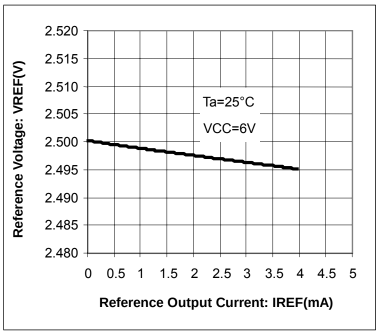


Fig.5 VREF current capability

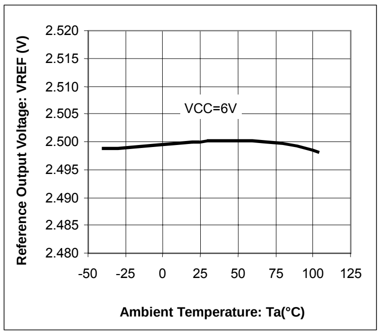


Fig.6 VREF temperature characteristics

● Reference data

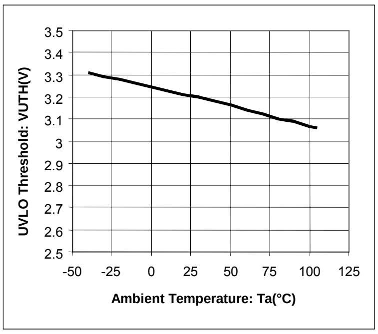


Fig.7 UVLO threshold temperature characteristics

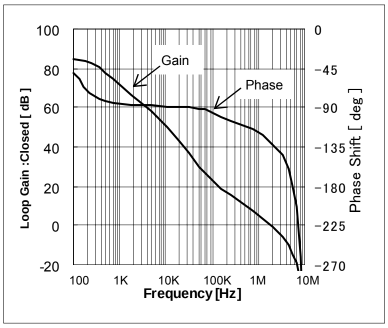


Fig.8 Error amplifier I/O characteristics

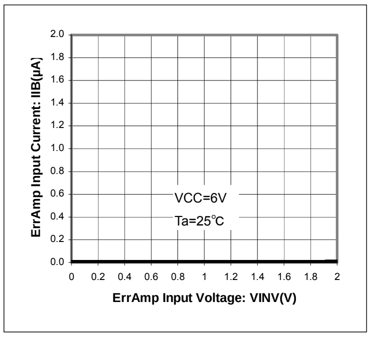


Fig.9 Error amplifier input current

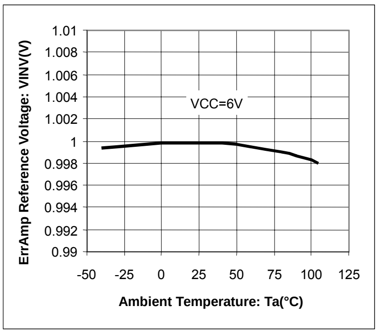


Fig.10 Error amplifier reference voltage temperature characteristics

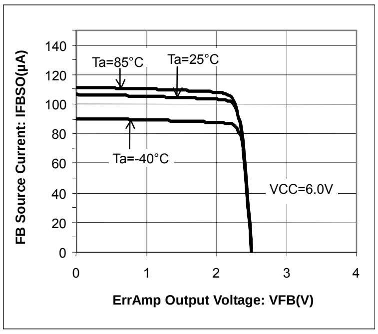


Fig.11 FB output source current

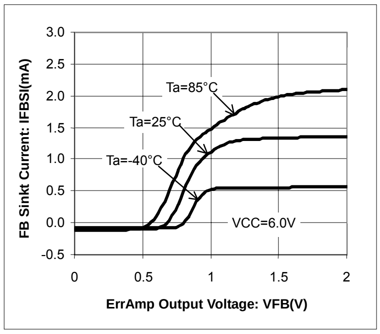


Fig.12 FB output sink current

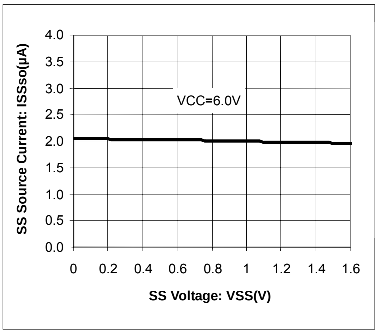


Fig.13 SS source current

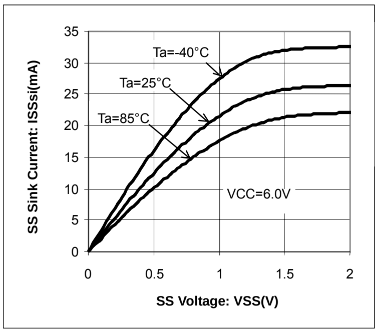


Fig.14 SS sink current

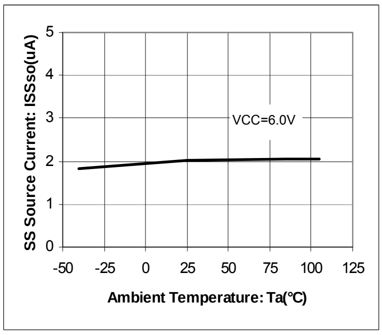


Fig.15 SS source current temperature characteristics

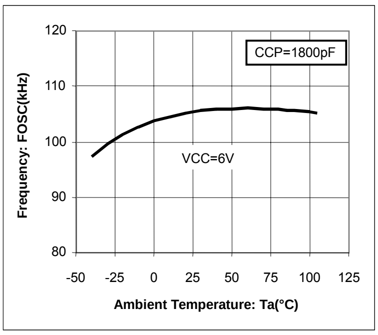


Fig.16 Oscillation frequency temperature characteristics

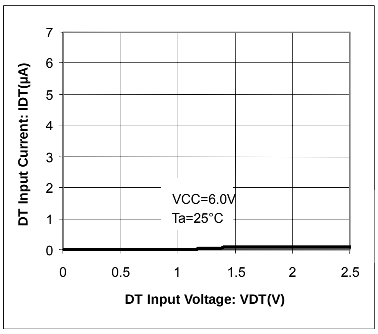


Fig.17 DT bias current

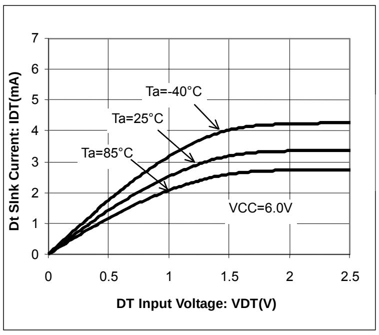


Fig.18 DT sink current

●Reference data

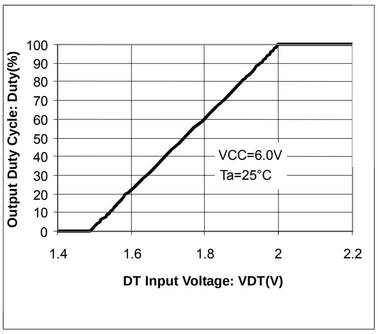


Fig.19 Output Duty-VDT characteristics (100kHz)

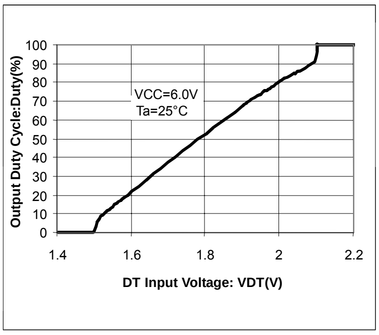


Fig.20 Output Duty-VDT characteristics (1.5MHz)

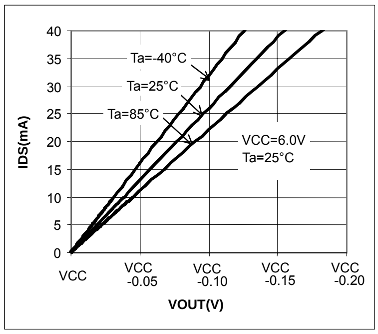


Fig.21 Output ON resistance H (RONH)

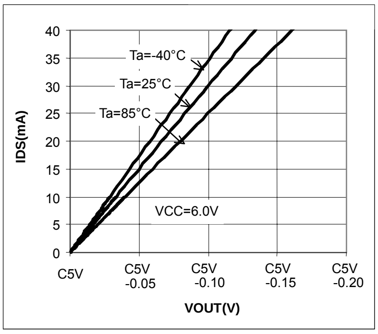


Fig.22 Output ON resistance L (RONH)

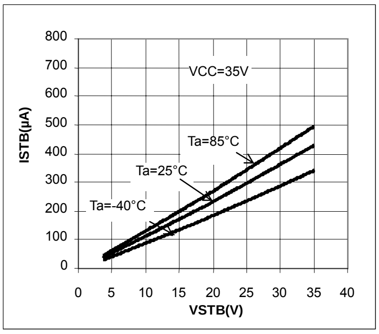


Fig.23 STB flow-in current

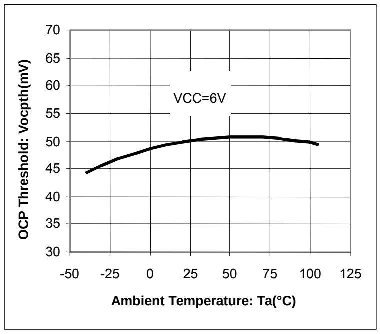


Fig.24 Overcurrent detection voltage temperature characteristics

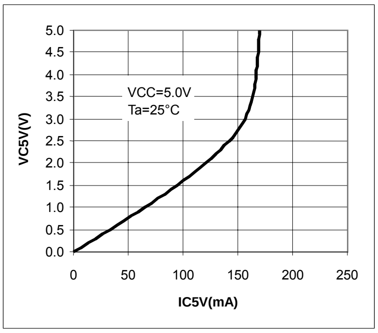


Fig.25 C5V saturation voltage

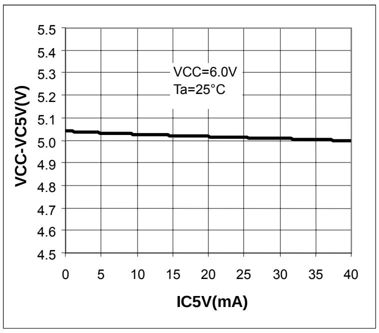


Fig.26 C5V load regulation

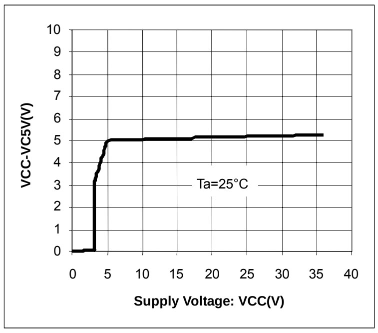


Fig.27 C5V line regulation

●Block diagram/Pin layout

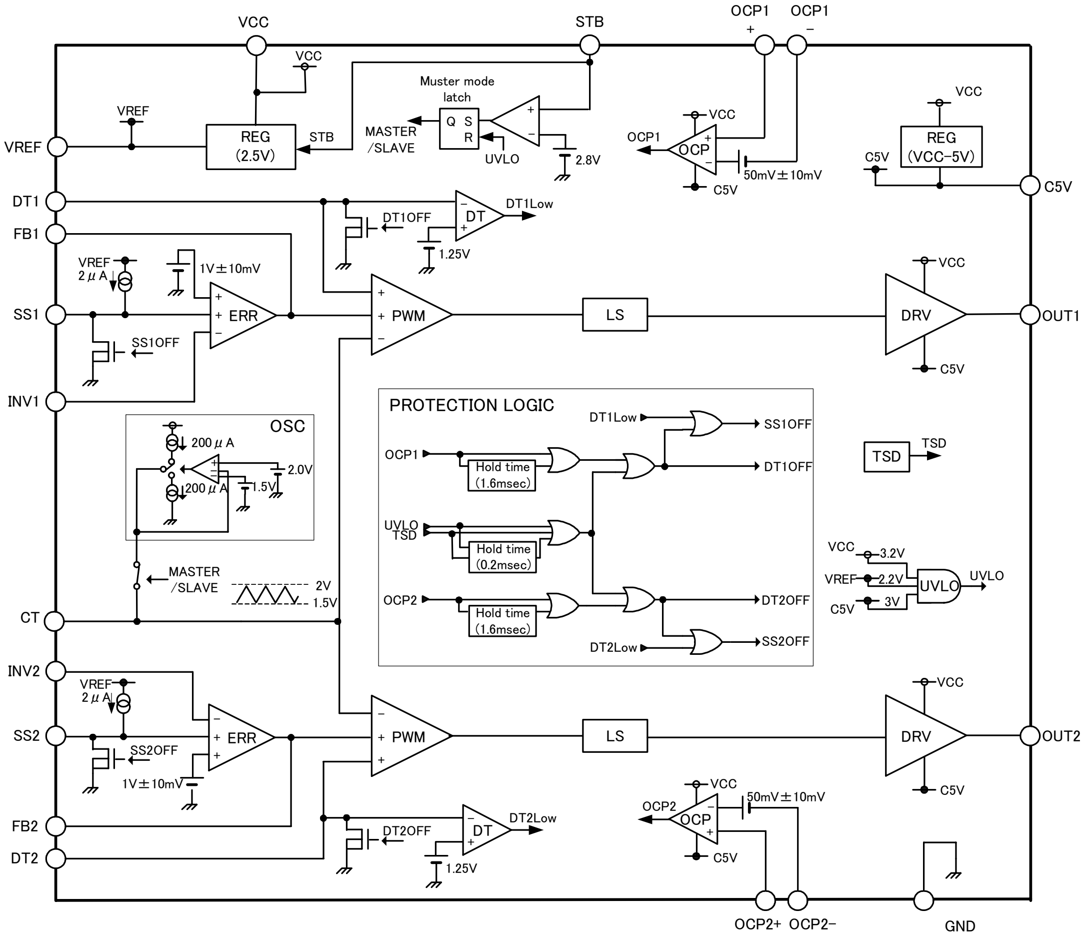


Fig.28 Block diagram

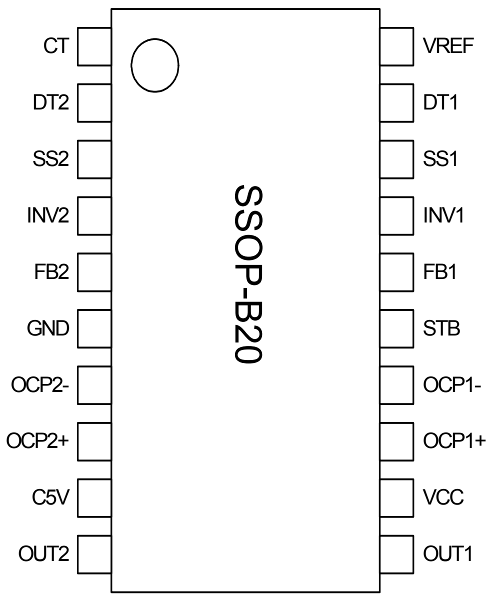


Fig.29 Pin layout

Terminal number	Terminal name	Function
1	CT	Timing capacity external terminal
2	DT2	Output 2 dead time setting terminal
3	SS2	Output 2 soft start time setting terminal
4	INV2	Output 2 error amplifier - input terminal
5	FB2	Output 2 error amplifier output terminal
6	GND	GROUND
7	OCP2-	Output 2 Overcurrent detector - input terminal
8	OCP2+	Output 2 Overcurrent detector + input terminal
9	C5V	Output L side voltage (Vcc-5V)
10	OUT2	Output 2
11	OUT1	Output 1
12	Vcc	Power terminal
13	OCP1+	Output 1 Overcurrent detector + Input terminal
14	OCP1-	Output 2 Overcurrent detector - Input terminal
15	STB	Standby mode setting terminal
16	FB1	Output 1 Error amplifier output terminal
17	INV1	Output 1 Error amplifier - input terminal
18	SS1	Output 1 Soft start time setting terminal
19	DT1	Output 1 Dead time setting terminal
20	VREF	Reference voltage (2.5V) output terminal

●Operation description of each block and function

1) REG (reference voltage unit)

As for REG (2.5V), reference voltage (2.5V) stabilized better than supply voltage input to VCC terminal (pin 12) is supplied as an operation voltage of IC internal circuit, as well as output outside through VREF terminal (pin 20). Insert a capacitor of 0.1 micro F to VREF terminal.

As for REG (VCC-5V), voltage of VCC-5V is supplied as power supply (LDO) of driver circuit (DRV) of OUT terminal (pin 10 and 11), as well as output outside through C5V terminal (pin 9). Insert a capacitor of 1 micro F to VCC terminal of C5V terminal.

2) ERR Amp 1/2 (error amplifier)

In step-down application, inverting input INV (pin 4 and 17) of error amplifier detects output voltage by sending back feedback current from final output stage (on load side) of switching regulator. R1 and R2 connected to this input terminal are resistor for setting output voltage. Non-inverting input of amplifier is a reference input of error amplifier itself by adding reference voltage (1.0V) inside IC.

Rf and Cf connected between FB (pin 5 and 16), which is output from error amplifier, and INV (pin 4 and 17) are for feedback of error amplifier, and allows setting of loop gain.

FB is connected to PWM Comp 1/2 and supplied as non-inverting input.

Setting of output voltage (Vo) is as follows:

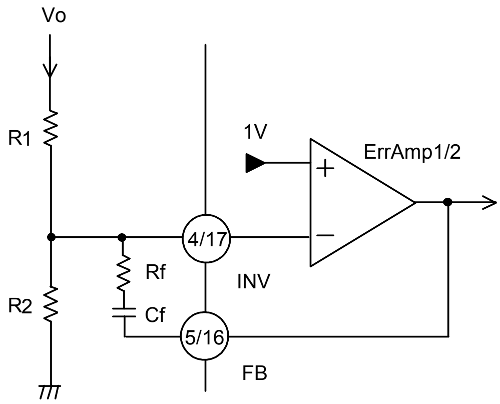


Fig.30

$$Vo = \frac{R1+R2}{R2} \times 1.0V$$

3) OSC (triangular wave oscillating unit)

Generates triangular wave for inputting to PWM Comp 1/2.

First, timing capacitor C_{CT} connected between CT terminal (pin 1) and GND is charged by constant current (200 micro A) generated inside IC. When CT voltage reaches 2.0 V typ, the comparator is switched, and then C_{CT} is discharged by constant current (200 micro A). Then, when CT voltage reaches 1.5V, the comparator is switched again, and C_{CT} is charged again. This repetition generates triangular wave.

Oscillation frequency is determined by externally mounted C_{CT} through theoretical formula below:

$$Fosc \fallingdotseq ICT/(2 \cdot C_{CT} \cdot \Delta Vosc)$$

ICT : CT sink/source current 200 micro A typ

ΔVosc : Triangular wave amplifying voltage＝(Vt0-Vt100)＝0.50 V typ.

Here, error from theoretical formula is caused by delay of internal circuit at a high frequency. See the graph in Fig 31 for setting.

This triangular wave can be taken out through CT terminal. It is also possible to input the oscillator externally by switching to slave mode described later. Waveform input here in principle must be triangular wave of Vpeak = (1.5V ⇔ 2.0V) equivalent to internal oscillation circuit.

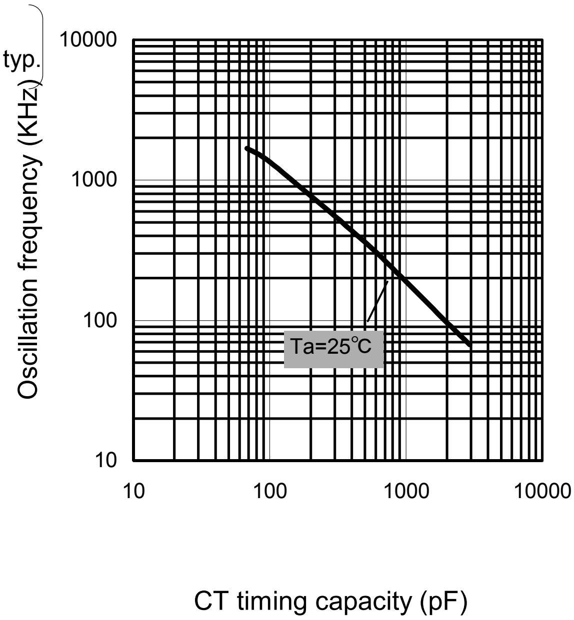


Fig.31

External input voltage range

V_{CT} : $1.4\ V < V_{CT} < 2.3\ V$

Standard external C_{CT} range

C_{CT} : MIN.47 pF – MAX.3000 pF

4) Soft start 1/2 (soft start function)

It is possible to provide SS terminal (pin 3 and 18) with soft start function by connecting C_{SS} as shown on the right.

Soft start time TSS is shown by the formula below:

$$Tss = Css \cdot \frac{Vinv}{Issso}$$

Css : SS terminal connection capacity
Vinv : Error amplifier reference voltage (1V typ)
Issso : SS source current (2 micro A typ)

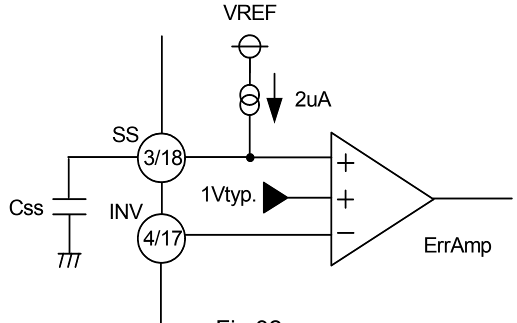


Fig.32

(Ex) When Css = 0.1 micro F

$$Tss = \frac{0.01 \times 10^{-6} \times 1}{2 \times 10^{-6}}$$

$$= 5 \text{ [msec]}$$

In order to function soft start, time must be set longer enough than start time of power supply and STB.

It is also possible to provide function of soft start by connecting the resistor (R1/R2) and capacitor (C_{DT}) to DT terminal (pin 2 and 19) as shown on the right.

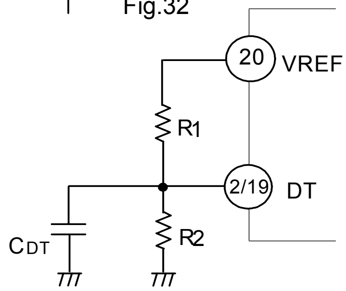


Fig.33

5) PWM Comp 1/2 - DEAD TIME (Pause period adjusting circuit - dead time)

Dead time can be set by applying voltage dividing resistance between VREF and GND to DT terminal (pin 2 and 19). PWM Comp compares the input dead time voltage (DT terminal voltage) and error voltage from Err Amp (FB terminal voltage) with triangular wave, and turns off and on the output. When dead time voltage < error voltage, duty of output is determined by dead time voltage. (When dead time setting is not used, pull up DT terminal to VREF terminal with resistor approx 10 k ohms.)

Dead time voltage VDT in Fig 32 is shown by the formula below:

$$VDT = VREF \cdot \frac{R2}{R1 + R2}$$

Relation between VDT and Duty [See the graph on the right.]

	Duty 100%			Duty 0%		
	min	typ	max	min	typ	max
When f = 100kHz	1.9	2.0	2.1	1.4	1.5	1.6
When f = 1.5MHz	1.95	2.1	2.25	1.35	1.5	1.65

[Unit : V]

When oscillation frequency is high, upper/lower limit of triangular wave (Vt100/Vt0) is shifted by delay time of comparator to directions expanding amplitude. Be careful.

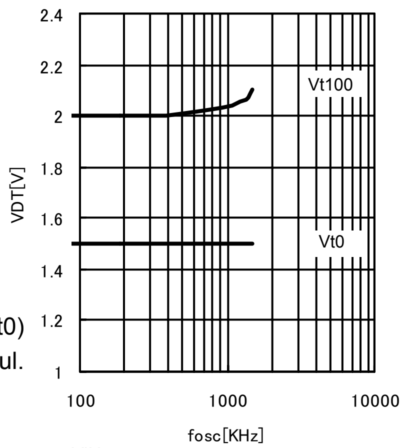


Fig.34

6) OCP Comp 1/2 (overcurrent detection circuit)

This function provides protection by forcibly turning off the output when abnormal overcurrent flows due to shorting of output, etc. When voltage between terminal OCP+(pin 8 and 13)/OCP-(pin 7 and 14) monitoring the current with sense resistor exceeds overcurrent detection voltage (50 mV typ), it is determined as overcurrent condition, and switching operation is stopped immediately by setting OUT to "H" and DT,SS (and FB) to "L".

It is automatically recovered when voltage between terminal OCP+/OCP- is below overcurrent detection voltage.

In addition, although hysteresis, etc. are not set here, minimum detection retention time (1.6mStyp) is set for suppressing the heating of FET, etc. (See the timing chart.)

When the overcurrent detection circuit is not used, short-circuit both terminal OCP+/OCP- to VCC pin.

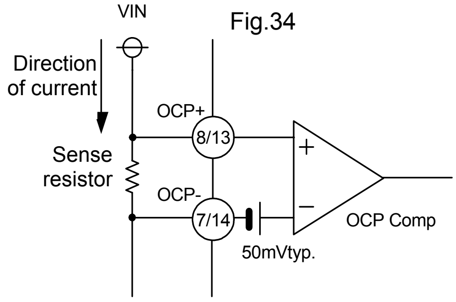


Fig.35

7) STB (Standby/Master/Slave function)

Standby mode, slave mode, and normal (master) mode can be switched by STB terminal (pin 15).

1. When STB<0.5V, standby mode is set.
   Output stops (OUT=H) and REG also stops. Circuit current is also Isc = 0 microA here.
2. When 2.4V<STB<2.6V, slave mode is set.
   Operation status is set, but OSC block alone is stopped, CT terminal is High-Z here, and triangular wave is not output. (PWM circuit and protection circuit perform the same operation as usual.) Therefore, if the controller is used in this mode without using master IC, triangular wave is not emitted, operation is unstable, and normal output cannot be obtained. Be careful.
3. When STB>3.0V, normal operation mode is set.
   All circuits operate and triangular wave is output. Use the controller normally in this range.

Precaution here is as follows:

When switching between standby mode and normal (master) mode, the current passes the area of slave mode.

When starting, if the time when 0.5V<STB<3.0V is long, the mode is switched with CT remaining unstable. Therefore start within a time when UVLO is canceled (within 100 microseconds approx.) for activation time of STB.

When falling, once normal (master) mode is set, normal (master) mode is fixed until UVLO operates, and it does not depend on falling speed of STB.

8) OUT 1/2 (Output: External FET gage drive)

OUT terminal (pin 10 and 11) is capable of directly driving the gate of external (PchMOS) FET. Amplitude of output is restricted between Vcc and C5V (Vcc 5V), and is not restricted by voltage resistance of gate by input voltage, which allows broad selection of FET.

However, for precaution when selecting FET, there is a restriction that input capacity of gate is determined by current capability of C5V and permissible loss of IC, therefore refer to the permissible range in the graph on the right when determining FET.

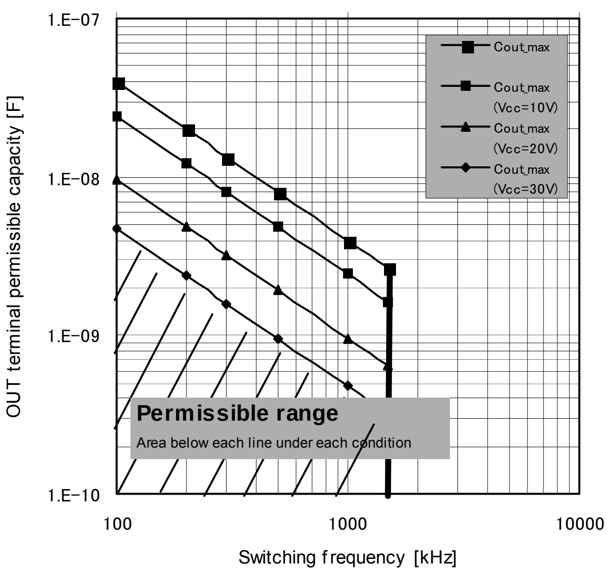


Fig.36

9) Protection (other protection functions)

This IC is equipped with low input malfunction prevention circuit (UVLO) and abnormal temperature protection circuit (TSD) in addition to overcurrent detection circuit (OCP).

Low input malfunction prevention circuit is for preventing unstable output when input voltage is low.

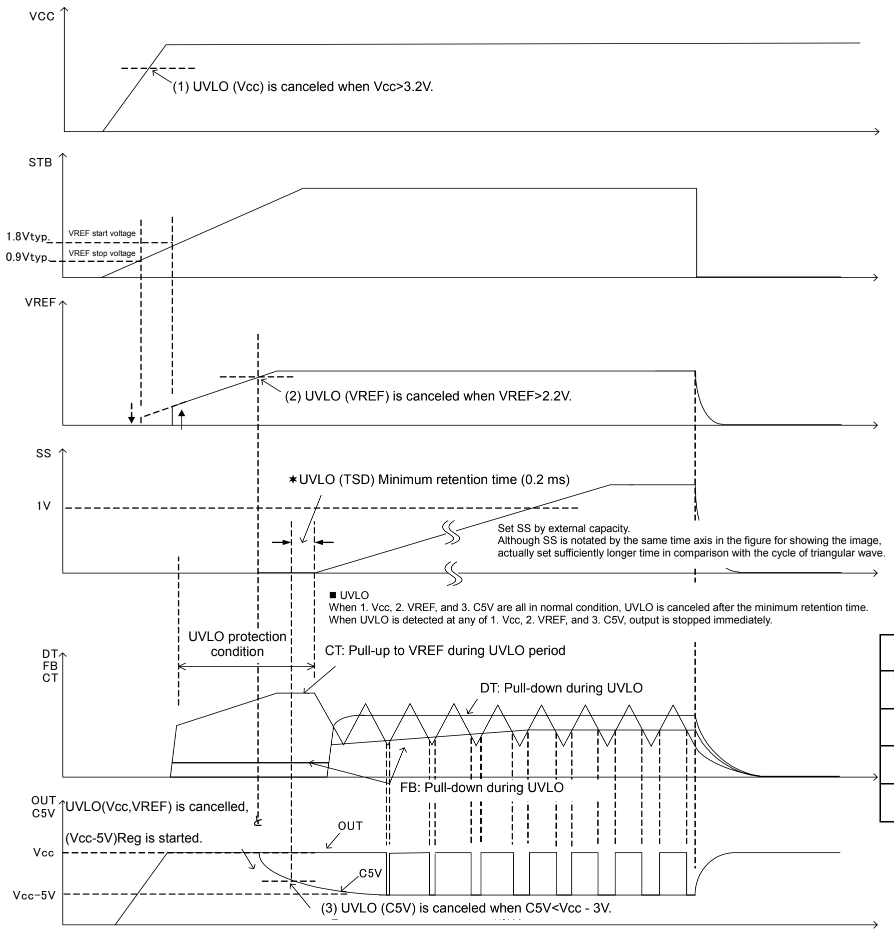
Three positions of Vcc (3.2V), VREF(2.35V), and C5V(Vcc-3V) are monitored, and output is made only when all are canceled. (See the timing chart.)

Abnormal temperature protection circuit is for protecting IC chip from destruction for preventing runaway when abnormal heating is caused on IC exceeding rated temperature. (It does not operate normally.)

Apply a design with full margin allowed for heating in consideration of permissible loss.

● Timing chart

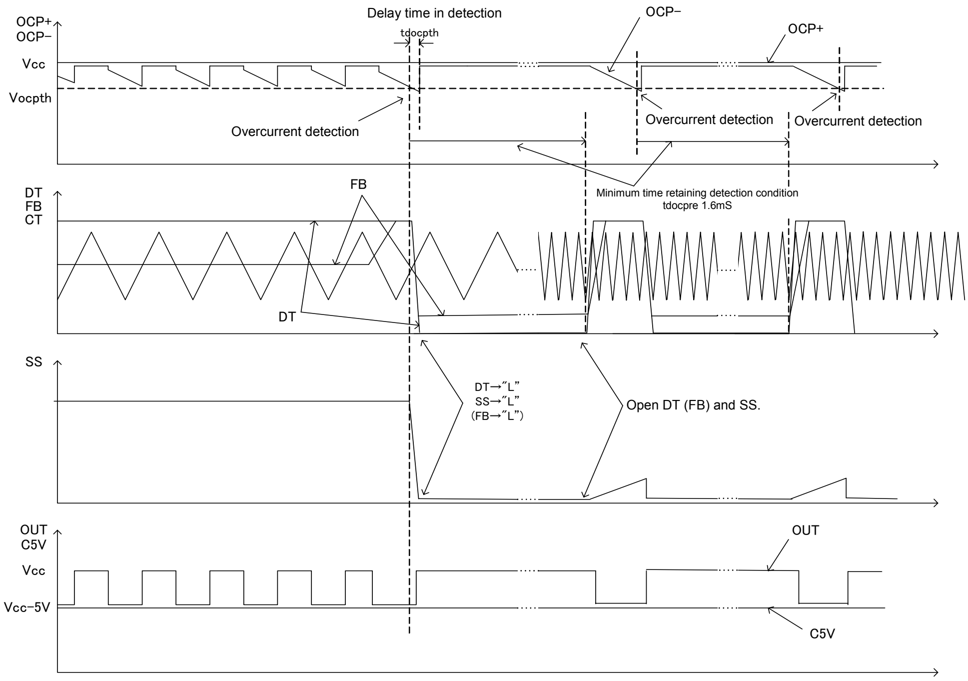
◎Starting characteristics (UVLO cancel) and standby operation



UVLO voltage [unit: V]

Item	Minimum	Standard	Maximum
Threshold voltage (VCC)	3.0	3.2	3.4
Hysteresis	-	0.15	0.25
Threshold voltage (VREF)	2.0	2.2	2.4
Threshold voltage (C5V)	-	3.0	3.4

◎Overcurrent detection (When output is shorted: Overcurrent detection and cancel are repeated at a specified time interval.)



●Example of application circuit

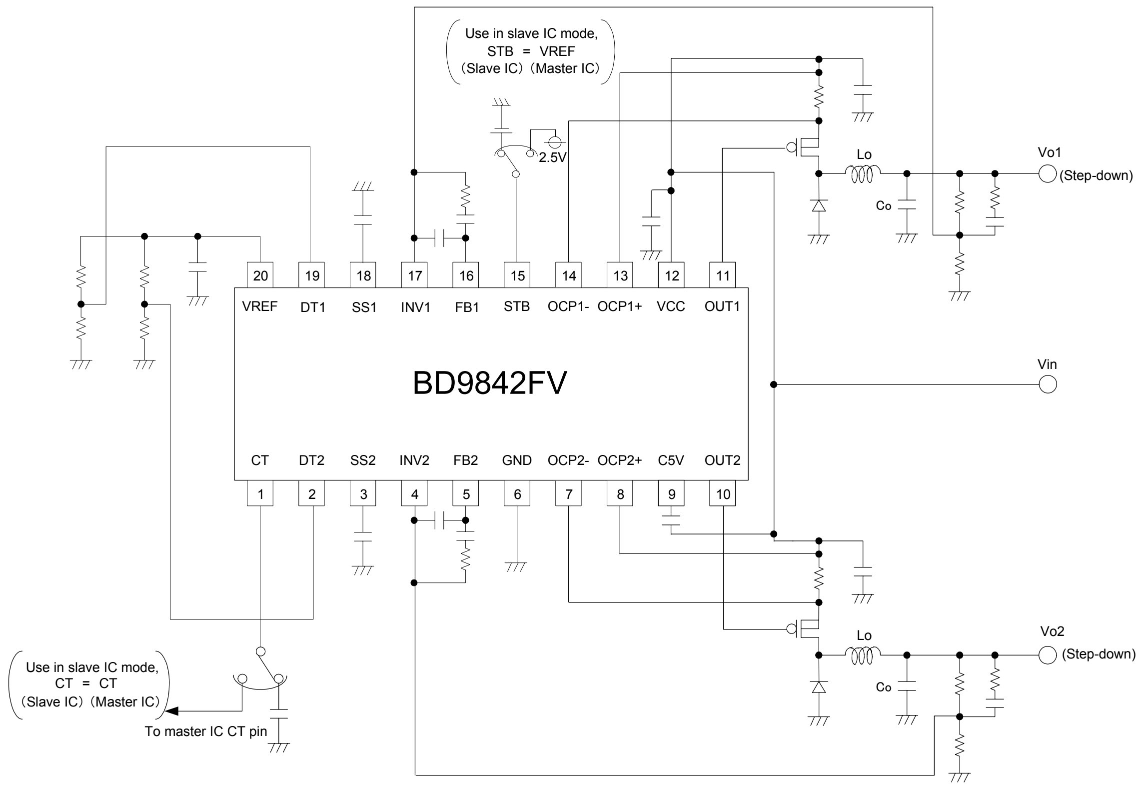


Fig.37

1) Setting of output unit coil (L) and capacitor (Co)

Set the coil and capacitor as follows in step-down application:

<Setting of L-value>

When load current gets heavy, the current flowing through the coil gets continuous, and the relation below is established:

$$L = \frac{Tsw}{\Delta IL} \times \frac{(Vin-Vo) \times Vo}{Vin}$$

Vin: Input voltage

Tsw: 1/(switching frequency)

Delta IL: Ripple current of coil

Normally set Delta IL below 30% of the maximum output current (Iomax).

When L-value is made greater, ripple current (Delta IL) becomes smaller. In general, the greater the L-value is, the smaller the permissible current of coil gets, and when the current exceeds permissible current, the coil is saturated and L-value changes. Contact the coil manufacturer and check permissible current.

<Setting of output capacitor Co>

Select an output capacitor Co by ESR (equivalent serial resistance) property of capacitor.

Output ripple voltage (Delta Vo) is almost ESR of output capacitor, therefore,

$$\Delta Vo \fallingdotseq \Delta IL \times ESR$$

ESR: Equivalent serial resistance of output capacitor Co

The relation above is established.

Ripple component by output capacitor is small enough to be neglected in comparison with ripple component by ESR in many cases. As for Co value, it is recommended to use a sufficiently large capacitor with a capacity that satisfies ESR condition.

<Switching element>

Determine a switching element by peak current. Peak current Isw <peak> flowing through the switching element is equal to peak current flowing through the coil, therefore the equation below is established.

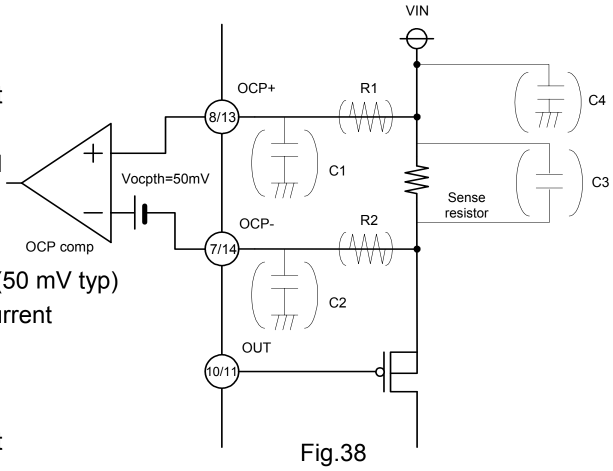
$$Isw\ (peak) = Io + \Delta IL/2$$

Select a switching element of permissible current having a sufficient margin over peak current calculated by the equation.

2) Example of overcurrent protection circuit

Insert a sense resistor between the source and VIN of output Pch-FET for detecting overcurrent as shown in the figure.

Refer to the formula below for determining a sense resistor and select permissible loss ensuring a margin.



$$Rsense = \frac{Vocpth}{Iocp}$$

Vocpth : Overcurrent detection voltage (50 mV typ)

Iocp : Overcurrent detection setting current

Fig.38

Iocp is a peak current Isw (peak) here, and the amperage for output load is an overcurrent setting amperage minus ripple current component (Delta I_L/2), etc. (See the formula on P10.)

There is a time delay approx 200ns from detection until stop of output is made (pulse of approx 100 ns causes delay time but detection is made), and an error may be caused from the value above.

In addition, input to overcurrent detection unit is such a sensitive circuit, and wrong detection by noise may be possible. When wrong detection occurs, try to eliminate noise by the resistor R1 and R2 or capacitance C1, C2, C3, and C4 shown above.

3) Example of output ON/OFF control circuit

When stopping the whole circuit, set STB terminal to "Low (STB<0.5V) to stop switching and reduce power consumption of IC to 0 microA (typ).

Also when switching ON and OFF for each channel, control is fixed to OFF by setting DT terminal of desired channel to "Low (DT<1.25V)". This control is independent for each channel, and when DT="L", SS terminal and FB terminal are also discharged, and soft start is enabled in restarting.

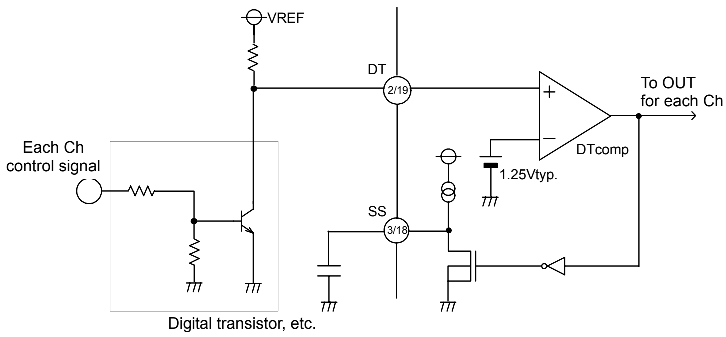


Fig.39

4) Example of master/slave (sync multi-ch output) operation circuit

This IC is set to slave mode by setting the input of STB terminal at 2.5V±0.1V, and multi-channel output is enabled with frequency synchronized. (Fig.40) However, CT terminal has high impedance in slave mode status, and triangular wave is generated by CT waveform of master mode IC. Therefore the example of master slave circuit below is recommended when starting and stopping in order to avoid malfunction by start/stop timing of master IC and slave IC. As for output, it is recommended to control ON/OFF reliably with DT terminal.

Also, oscillation frequency is determined by capacitor (C_{CT}) connected to CT. When the slave IC is large in number as well as oscillation frequency is high, parasitic capacity by board wiring in contact with CT cannot be ignored, and preset frequency may be drifted. Be careful.

Example of master/slave circuit configuration is shown below. If any other configuration is to be applied, inform our personnel in charge.

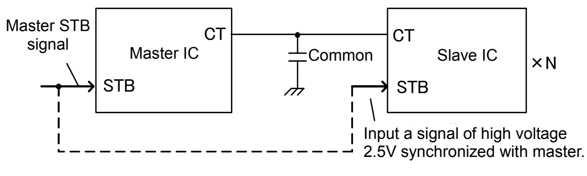


Fig.40

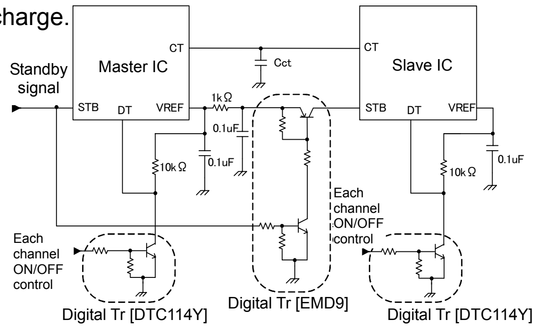


Fig 41. Example of master/slave 1

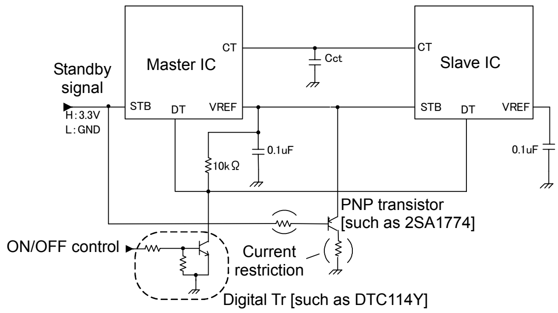


Fig 42. Example of master/slave 2

5) About board layout

In order to make full use of IC performance, fully investigate the items below in addition to general precautions.

- Each output of OCP+/OCP- is such a sensitive circuit. When wiring is routed around, it is easily subjected to noise. Try to make the wiring as short as possible.
- Switching of large current is likely to generate noise. Try to make the large current route (VIN, Rsense, FET, L, Di, and Cout) as thick and short as possible, and try to apply one-point grounding for GND. OUT terminal is also a switching line, and it must be wired along a distance as short as possible. (When multi-layer board is used, shielding by intermediate layer also seems to be effective.)
- C_{CT} and C_{VREF} are reference of all, and must be wired along the shortest distance to GND of IC stabilized to be protected against external influence.
- Also be careful not to allow common impedance to sense family GND.

(6) PIN processing of channel unused

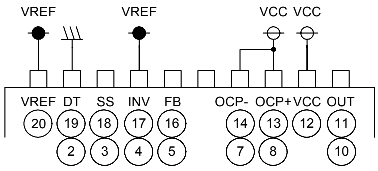
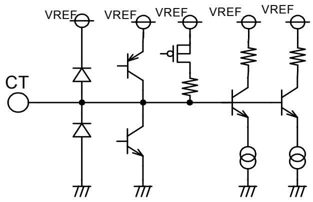
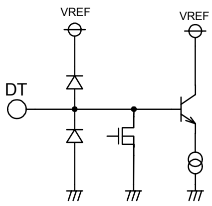
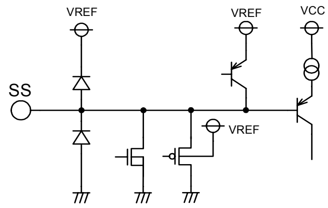
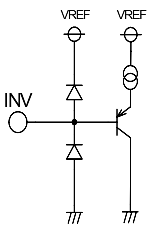
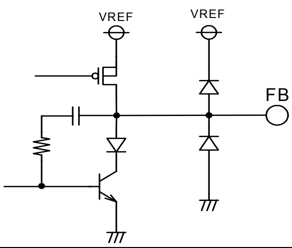
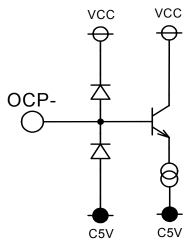
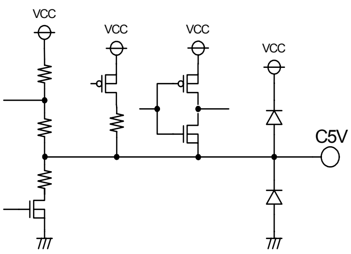
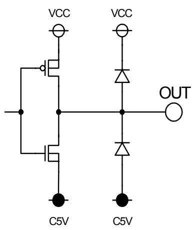
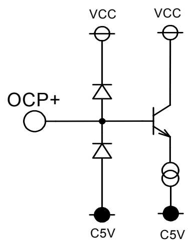
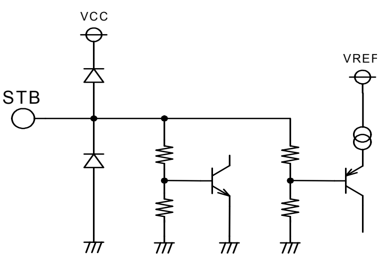
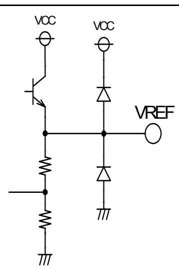
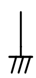


Fig.43

When only one channel is used, process unused channels as shown above.

●I/O equivalent circuit diagram

Pin 1 (CT)	Pin 2, and 19 (DT1 and DT2)	Pin 3, and 18 (SS1 and SS2)	
			
Pin 4, and 17 (INV1 and INV2)	Pin 5, and 16 (FB1 and FB2)	Pin 7, and 14 (OCP1- and OCP2-)	
			
Pin 9 (C5V)	Pin 10, and 11 (OUT1 and OUT2)	Pin 8, and 13 (OCP1+ and OCP2+)	
			
Pin 15 (STB)	Pin 20 (VREF)	Pin 6 (GND)	Pin 12 (VCC)
		 GND	VCC 

● Precaution for use

1) About maximum absolute rating
When the maximum absolute rating of application voltage or operation voltage range is exceeded, it may lead to deterioration or rupture. It is impossible to forecast rupture in short mode or open mode. When a special mode is expected exceeding the maximum absolute rating, try to take a physical safety measure such as a fuse.

2) GND potential
Ensure that the potential of GND terminal is the minimum in any operation condition. Also ensure that no terminal except GND terminal has a voltage below GND voltage including actual transient phenomenon.

3) Thermal design
Allow a sufficient margin in thermal design in consideration of permissible loss (Pd) in actual use condition.

4) Shorting between terminals and wrong attachment
When attaching an IC to a set board, pay full attention to the direction of IC and dislocation. Wrong attachment may cause rupture of IC. In addition, when shorting is caused by foreign substance placed between outputs or between output and power supply-GND, rupture is also possible.

5) Operation in intense magnetic field
Use in intense magnetic field may result in malfunction. Be careful.

6) Inspection on set board
In inspection on set board, when a capacitor is connected to a terminal with low impedance, stress may be applied to IC, therefore be sure to discharge electricity in each process. Apply grounding to assembling process for a measure against static electricity, and take enough care in transport and storage. When connecting a jig in inspection process, be sure to turn off power before detaching IC.

7) About IC terminal input
This IC is a monolithic IC, and contains P^+ isolation and P board for separating elements between each element. This P-layer and N-layer of each element form P-N junction, and many kinds of parasitic elements are constituted. (See Fig 43.)
For example, when resistor and transistor are connected with a terminal as shown below.
○ P-N junction operates as a parasitic diode when GND>(Terminal A) for resistor, and when GND>(Terminal B) for transistor (NPN).
○ In addition, when GND>(Terminal B) for transistor (NPN), parasitic NPN transistor is operated by N-layer of some other elements in the vicinity of parasitic diode mentioned above.
Parasitic element is inevitably generated by potential because of IC structure. Operation of parasitic element causes interference with circuit operation, and may lead to malfunction, and also may cause rupture. Therefore when applying a voltage lower than GND (P board) to I/O terminal, pay full attention to usage so that parasitic elements do not operate.

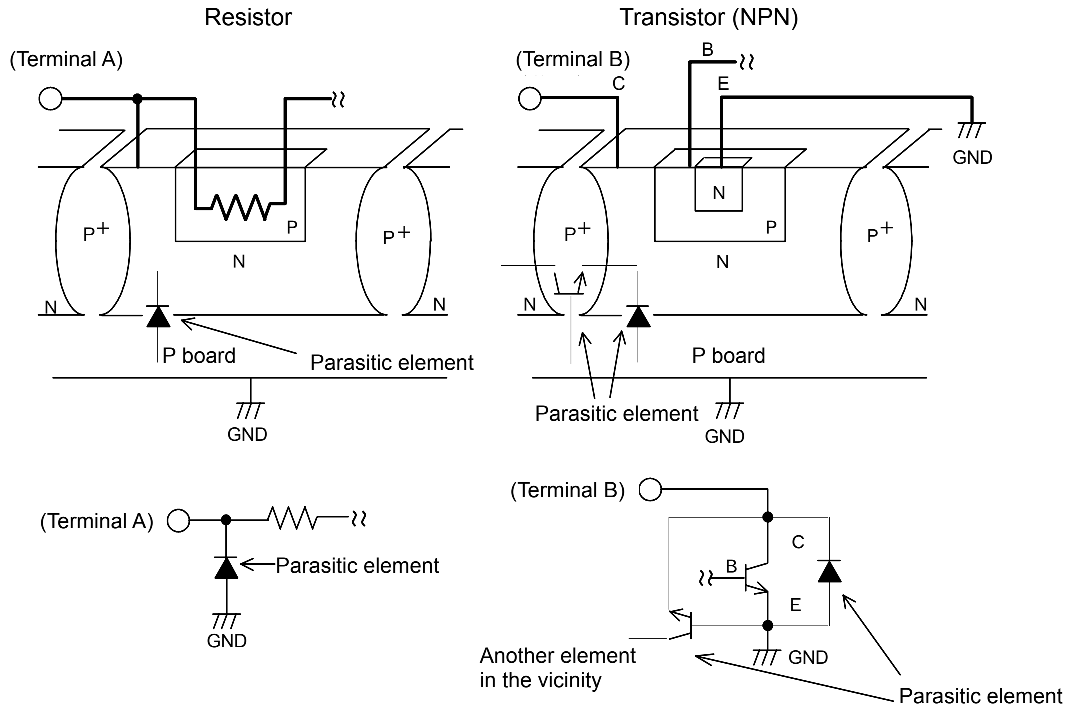
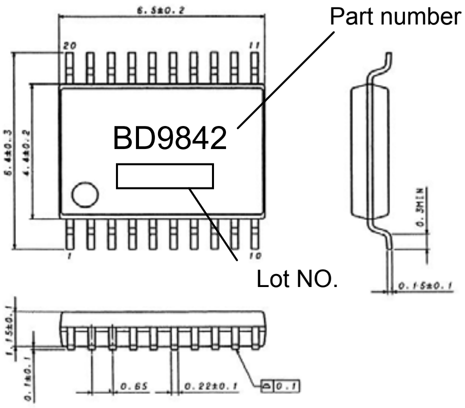


Fig.44

● Outer dimension view

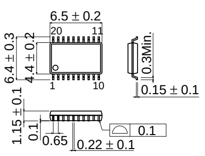


●Order model name

BD	9842	FV	—	E2
ROHM model name	Part number	Package type FV=SSOP-B20		Taping model name E2 = Reel-shape emboss taping

SSOP-B20

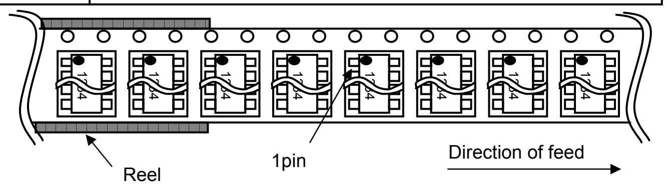
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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